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CLAIMS:

1. A semiconductor device having a first and an opposite second side, comprising:
- a substrate comprising a semiconductor layer and an electrically insulating layer, and being present on the first side of the device;
 - 5 - an integrated circuit provided with a plurality of semiconductor elements, which are defined in and/or on the semiconductor layer and are interconnected according to a desired pattern in an interconnect structure;
 - a first contact face that is present on the first side of the device;
 - a second contact face that is present on the second side of the device, and is
 - 10 connected to the interconnect structure;
- wherein:
- an electrically insulating support layer is present, which covers on the second side the integrated circuit and extends laterally around the integrated circuit in a non-active area, through which support layer a vertical interconnect is present to connect the second
 - 15 contact face with the interconnect structure;
 - the semiconductor layer of the substrate is laterally partially removed so as to be absent in the non-active area; and
 - the first contact face is connected to the interconnect structure through a
 - 20 vertical interconnect.
2. A semiconductor device as claimed in claim 1, characterized in that the vertical interconnect to the first contact face is present in the non-active area, the first contact face being defined in an electrically conducting layer.
- 25 3. A semiconductor device as claimed in claim 1 or 2, characterized in that the electrically insulating layer is laterally substantially continuous so as to be present in the non-active area.

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4. A semiconductor device as claimed in claim 1, characterized in that the interconnect structure is provided with a first and a second via pad, which are present in the non-active area, and at which pads the first and the second vertical interconnects respectively are present.
5. A semiconductor device as claimed in claim 4, wherein the via pads are present on the electrically insulating layer that is part of the substrate.
6. A semiconductor device as claimed in claim 4 or 5, characterized in that the second via pad and the second vertical interconnect comprise a ductile material.
7. A semiconductor device as claimed in claim 1, characterized in that the support layer comprises an organic material.
8. An identification label comprising the semiconductor device according to any of the claims 1 to 7 and an antenna for wireless transmission.
9. An information carrier comprising the semiconductor device according to any of the claims 1 to 7.
10. A method of manufacturing a semiconductor device comprising the steps of:
- providing a substrate with a semiconductor layer and an electrically insulating layer, an integrated circuit provided with a plurality of semiconductor elements being defined in an active area, the semiconductor elements being mutually interconnected according to a desired pattern in an interconnect structure, which interconnect structure comprises a first and a second via pad, which via pads are present in an area that is laterally substantially outside the active area;
 - applying a support layer of an electrically insulating material on the second side and providing a contact window in the support layer corresponding to the second via pad;
 - applying electrically conductive material in a desired pattern on the second side, therewith providing a second contact face and a second vertical interconnect between said contact face and the second via pad;

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- attaching the substrate on its second side to a carrier with removable attaching means;

- thinning the substrate from the first side, so that the insulating layer of the substrate is exposed at least in some non-active areas laterally outside and around the active area;

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- providing a first contact face on the first side, which is connected to the first via pad through a first vertical interconnect extending at least through the insulating layer; and

- removing the thus obtained semiconductor device from the carrier.

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11. A method as claimed in claim 10, wherein the oxide layer is buried inside the semiconductor substrate, the substrate further comprising a base layer and an active layer, which base layer is removed in the thinning step and on a surface of which active layer the semiconductor elements are defined.

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12. A method as claimed in claim 10, wherein the first vertical interconnect is provided as part of the integrated circuit.